DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 09/15/2009 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 5-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Chen (US 2003/0143772).

Regarding claim 5, Chen discloses a method for manufacturing a compound semiconductor substrate, comprising the steps of: (f) epitaxilaly growing a compound semiconductor functional layer (Fig.6A, numerals 102-119) on a substrate (Fig.6A, numeral 100), (g) bonding a thermally conductive substrate (Fig.6B, numeral 125; Fig.6C) having a thermal conductivity higher than that of the substrate (Fig.6A, numeral 118)) to the surface of the compound semiconductor functional layer ([0028]) and (h)

polishing the substrate and a part of the compound semiconductor functional layer on the side which is in contact with the substrate to remove them ([0030]).

Regarding claim 6 Chen discloses the compound semiconductor functional layer includes at least two layers (Fig.6A).

Regarding claim 7, Chen discloses that the compound semiconductor functional layer includes at least one selected from the group consisting of In, Ga, and Al and at least one selected from the group consisting of N, P, and As [0023]-[0025]).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 1-3, and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mori (JP 6-349731) in view of Greskovich (US 4, 040, 849).

Regarding claim 1, Mori discloses epitaxilaly growing a compound semiconductor functional layer (Fig.4a, numerals 21,32,6,3), on a substrate (Fig.4a, numeral 4); bonding a support substrate (Fig.4c, numeral 41) to the compound semiconductor layer (paragraph [0058]); polishing the substrate and a part of the compound functional semiconductor layer on the side which is in contact with the substrate, to remove them (Fig.4c; paragraph [0058])); bonding a thermally conductive substrate (Fig.4D, numeral 1, paragraph [0059]) having a thermal conductivity higher than that of substrate (4)

(note: substrate (4) is InP, [0054], and substrate (1) is Si) to the exposed surface of the compound semiconductor functional layer (3) to obtain a multilayer substrate and separating the support substrate (41) from the multilayer substrate (Fig.4e, [0060]).

Mori does not disclose that the thermally conductive substrate includes at least one selected from the group consisting of a polycrystalline Si substrate obtained by CVD ,or sintering process; a substrate formed with a polycrystalline or amorphous diamond thin film having a thickness of about not more than 300 μm and about not less than 50 μm on a single crystal Si substrate, polycrystalline Si substrate or ceramics substrate; and a polycrystalline or amorphous SiC, AIN, and BN obtained by CVD or sintering process.

Mori however discloses that the thermally conductive substrate is an inexpensive Si substrate ([0002]). And Greskovich discloses that manufacturing polycrystalline silicon substrates by sintering allows one to obtain an inexpensive support material (column 1, lines 10-60).

It would have been therefore obvious to one of ordinary skill in the art at the time the invention was made to modify Mori with Greskovich to have a thermally conductive substrate from polycrystalline Si obtained by sintering for the purpose of decreasing cost of manufacturing.

Regarding claim 2, Mori discloses that the compound semiconductor functions layer includes at least two layers (Fig.4a, 21,32, 6, 3).

Regarding claim 3, Mori discloses that the compound semiconductor functional layer includes at least one selected form the group consisting of In, Ga and at least one selected form the croup consisting of N and As [0054]).

Regarding claim 9, Mori does not disclose a step of forming an electrode on the resultant compound semiconductor device.

It would have been however obvious to one of ordinary skill in the art at time the invention was made to form an electrode on the resultant compound semiconductor devices for the purpose of using this structure as a light emitting diode.

6. Claims 1-3 and 9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong (US 7, 547, 925) in view of Sano (US 6, 916, 676), Wong'648 (US 652, 648) and Panchula ("Nanocrystalline Aluminum Nitride: II Sintering and Properties," J.A.Ceram. Soc. 86, 2003, pp.1121-1127).

Regarding claim 1, Wong discloses method for manufacturing a compound semiconductor substrate, comprising the steps of: (a) epitaxilaly growing a compound semiconductor functional layer (Fig.8A, numerals 14, 16, 52) on a substrate (Fig. 8A, numeral 12), (b) bonding a support substrate (Fig.8B, numeral 70) to the compound semiconductor functional layer (Fig.8B (numerals 52, 26, 24), (d) bonding a thermally conductive substrate (Fig. 8E, numeral 74) to the exposed surface of the compound semiconductor functional layer (2) which is provided in the step (c) to obtain a multilayer substrate (Fig.8E), and (e) separating the support substrate (Fig.8F, numeral 70) from the multilayer substrate (column 7, lines 50-55).

Wong does not disclose (1)polishing the substrate and a part of the compound semiconductor functional layer on the side which is in contact with the substrate to remove them; (2) that the thermal conductivity of the thermally conducting substrate is higher than that of a substrate; (3) that the thermally conductive substrate includes at least one selected from the group consisting of a polycrystalline Si substrate obtained by CVD ,or sintering process; a substrate formed with a polycrystalline or amorphous diamond thin film having a thickness of about not more than 300 μm and about not less than 50 μtm on a single crystal Si substrate, polycrystalline Si substrate or ceramics substrate; and a polycrystalline or amorphous SiC, AIN, and BN obtained by CVD or sintering process.

Regarding element (1), Wong discloses that the sapphire substrate and the part of a functional layer and are removed (Fig. 8C, numerals 12, 14). And Sano discloses the method of removing the sapphire substrate and the part of a functional layer by polishing (column 25, lines 14-26).

It would have been therefore obvious to one of ordinary skill in the art at the time the invention was made to modify Wong with Sano to polish the substrate and a part of the compound semiconductor functional layer on the side which is in contact with the substrate for the purpose of effective removing of the substrate and adjust the thickness of the nitride semiconductor layer and surface roughness (Sano, column 25, lines 15-26).

Regarding element (2), Wong discloses attaching the thermally conductive substrate (AIN) having a thermal conductivity higher than that of sapphire to LED device

(column 4, lines 62-67). And Wong'648 discloses that attaching the substrate having a thermal conductivity higher than that of the sapphire substrate allows one to reduce the thermal impedance and consequently reduces any thermal cross-talk (column 2, lines 11-45).

It would have been therefore obvious to one of ordinary skill in the art at the time the invention was made to modify Wong with Wong'648 to have the thermal conductivity of the thermally conducting substrate is higher than that of a substrate for the purpose of reducing any thermal cross-talk (Wong'648, column 2, lines 11-45).

Regarding element (3), Wong discloses that the thermally conductive substrate is AlN (column 4, lines 65-67). And Panchula discloses that forming polycrystalline AlN by sintering allows one to obtain AlN with good thermal conductivity (Panchula, abstract).

It would have been therefore obvious to one of ordinary skill in the art at the time the invention was made to modify Wong with Panchula to have the thermally conductive substrate made from polycrystalline AlN obtained by sintering for the purpose of obtaining substrate with good thermal conductivity (Panchula, abstract).

Regarding claim 2, Wong discloses that the compound semiconductor functional layer includes at least two layers (Fig.8A).

Regarding claim 3, Wong discloses that the compound semiconductor functional layer includes at least one selected from the group consisting of In, Ga and Al and at least one selected from the group consisting of N (Fig.8A).

Regarding claim 9, Wong discloses forming an electrode on the resultant compound semiconductor substrate (Fig.2E, numeral 54).

Response to Arguments

7. Applicant's arguments with respect to claims 1-3, 5-7, and 9 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to JULIA SLUTSKER whose telephone number is (571)270-3849. The examiner can normally be reached on Monday-Friday, 8 a.m.-5 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Keisha Bryant can be reached on (571)-272-1844. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

9. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic

Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JS
October 15, 2009

/Asok K. Sarkar/
Primary Examiner, Art Unit 2891
October 16, 2009